kandou

Regli PCIe® Retimer
KB9003

PCIe 5.0 32 GT/s and CXL™ 2.0 retimer, x16 bidirectional lanes

KB9003
Block Diagram
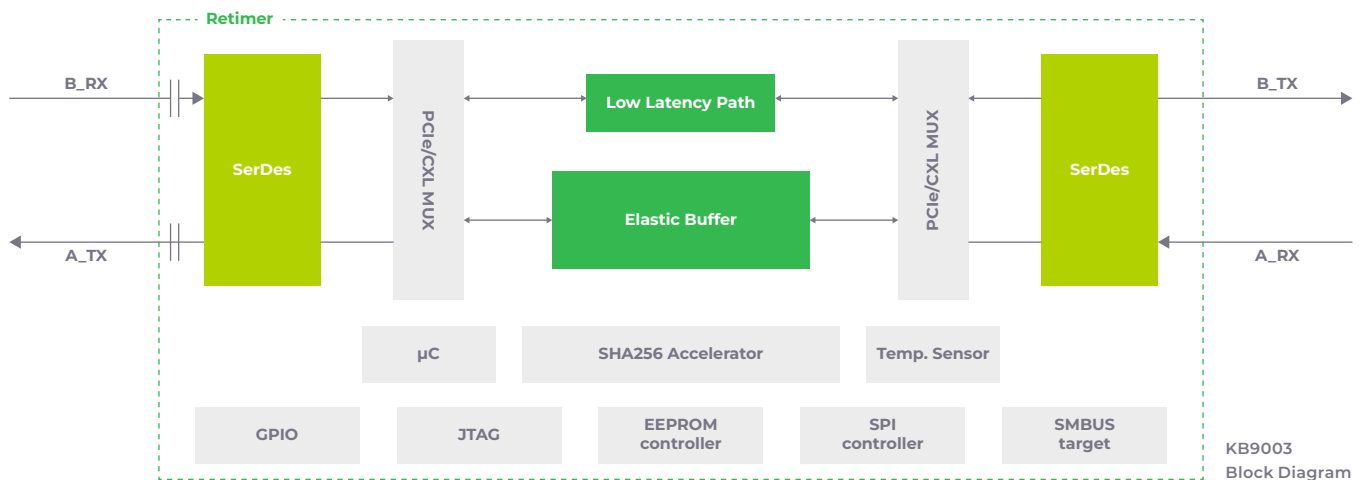
Product Overview:

▶ A 16-lane bidirectional PCIe® 5.0 and CXL™ 2.0 protocol-aware retimer that supports data rates up to 32 GT/s.

▶ Backwards compatible with PCIe 4.0/3.0/2.0/1.0.

▶ Dynamically compensates channel loss up to 36 dB. This allows designers to increase the PCIe trace length between a root complex and an endpoint while maintaining signal integrity as per the PCI-SIG specification.

▶ Supports CXL Retiming Mode, a common clock mode with different packet sizes and low-latency datapath mode or low-latency applications.

▶ Supports an integrated microcontroller (MC) for debug and firmware upgrades.

▶ Integrated microcontroller and SHA256 accelerator enabling secure boot at the platform to prevent attackers from altering the sideband boot configuration stored in an external SPI flash or EEPROM.

Features

PCIe 5.0 support

▶ Supports 2.5, 5, 8, 16, and 32 GT/s

▶ Retiming Mode: Up to MAX packet size (4096 B)

▶ Common clock with or without SSC and SRNS modes

▶ Ultra-low latency cut-through mode

▶ Link bifurcation support for x16, x8, x4, and x2

CXL 2.0 support

▶ Sync header bypass

▶ Enhanced LTSSM to handshake with CXL command

▶ Drift Buffer Mode (low latency bypass)

Extended system reach

▶ RX: Up to 36 dB @ 16 GHz Nyquist using adaptive EQ

Ultra-low latency

- CXL 2.0: 10 ns TYP
- PCIe 5.0 (Bypass Mode): 10 ns TYP
- Power Saving Mode: VDD_PWR12 (1.2 V)

Multiple control interface

- SMBus target or I2C target (BMC connection)
- EEPROM controller
- SPI controller (SPI flash)
- GPIO strapping pins for lane bifurcation configuration
- JTAG: support for JTAG 1149.1 and 1149.6

Flexible clock modes

- Integrated Clock Forward Mode buffer
- PCIe REFCLK and REFCLK_OUT (100 MHz)
- Common clock with or without SSC

Secure platform boot support

- OTP for public key (RSA-2048) storage
- Integrated SHA256 accelerator
- Integrated microcontroller

Integrated debug and error reporting

- Integrated EyeScope
- Integrated BER monitors
- Integrated logic analyzer
- Multiple loopback modes with PRBS pattern generation

Power supply

- VDD_PWR1:   1.8V
- VDD_PWR12: 1.8 V (Regular Mode), or 1.2 V (Power Saving Mode)
- VDD_PWR2:   0.9 V

Other

- Integrated AC coupling capacitors
- Ability to force presets during link training

Applications

- Servers, workstations and desktops
- Hyperscalers and data centers
- AI accelerator modules
- 5G infrastructure equipment
- CXL storage and memory
- PCIe storage
- PCIe riser cards, midplane and backplane

Device information

Ordering code	Package	Delivery form
KB9003-AD	BGA 8.9 x 22.8 mm 354-ball	Tray
KB9003-AR	BGA 8.9 x 22.8 mm 354-ball	Tape & reel
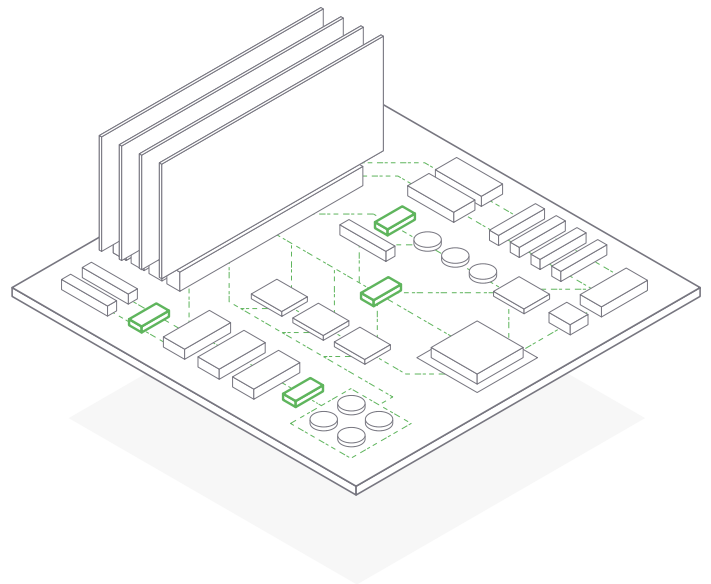
For ordering or more information, contact sales@kandou.com
www.kandou.com