Glasswing®
GW12-500-USR
Ultra-short reach SerDes with 500 Gbit/s throughput

The Glasswing family is a set of configurable PHY IPs designed and optimized for in-package applications that do not require a silicon interposer.

GW12-500-USR provides 500 Gbit/s of full-duplex system bandwidth at a power consumption as low as 1 pJ/bit, through the use of CNRZ-5 Chord™ Signaling and a forwarded clock architecture. Glasswing IP may be deployed in multiple instances to provide efficient extended interfaces.

Benefits
- 2x to 4x throughput at 50% or less energy consumption as compared to conventional SerDes over the same number of pins/wires
- High pin-efficiency and low power
- 208.3 Gbit/s full-duplex bandwidth per mm of die edge (500 Gbit/s for 2.4 mm of die edge)
- Supports up to 6 dB channel insertion loss at 12.5 GHz
- NRZ-like ISI and noise performance

Technology
- GlobalFoundries® 12LP process
- 0.9V and 1.2V analog supplies
- 0.8V digital supply
- Junction temperature -40°C to +110°C
- Standard flip chip technology with 150 μm bump pitch
- Tile-able layout to support high IO density

Features
- MCM interface consisting of four 6-wire CNRZ-5 Chords, plus a shared forwarded clock (26 wires total per direction)
- No silicon interposer required due to standard 150 μm bump pitch
- Maximum throughput of 500 Gbit/s in each direction
- Line rate programmable from 12.5 to 25 Gbd for a throughput of 62.5 to 125 Gbit/s per Chord
- Total throughput configurable by selecting number of active Chords
- TX and RX data buses consisting of five 32-bit data words (plus clock) for each Chord
- Simple word-based TX to RX interface, RX logic recovers data alignment
- DC-coupled link with no coding/framing requirements; light-weight scrambler in PMA Soft IP ensures sufficient data toggling
- Configuration and link start-up through APB (ARM Peripheral Bus) interface
Applications

- Multi-chip modules and short reach interposes:
  - Packaging dies with dissimilar foundry processes
  - Packaging of smaller dies to increase yield
- High throughput data interfaces:
  - Efficient interface to off-board SerDes tiles
  - Interconnection of tiled CPUs or DSPs
  - Processor or switch to high bandwidth memory
  - Efficient interface to optics engines
- Switch-to-switch links

CNRZ-5 Coding

- Transmits 5 bits on 6 correlated wires:
  - Balanced code leads to low SSO noise at transmitter
  - Employs a reference-less receiver that is resilient to common-mode noise
  - Uses a receiver that has five comparators and no decoder
- Link has excellent signal integrity properties:
  - NRZ-like ISI properties
  - Scalable to much higher speeds and harder channels
  - NRZ-like EMI performance

Deliverables

- Datasheet and application notes
- Hard IP standard integration views: LEF, LIB, SDC, GDSII, LVS netlist, ATPG netlist
- PMA Soft IP
- Verilog Hard IP customer model for system simulation: reference test bench
- Qualification report
- Package design and integration guidelines

For ordering or more information, contact sales@kandou.com
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