KA-009565-PB-6f76539

Regli PCIe® Retimer KB9003

PCIe 5.0 32 GT/s and CXL™ 2.0 retimer, x16 bidirectional lanes

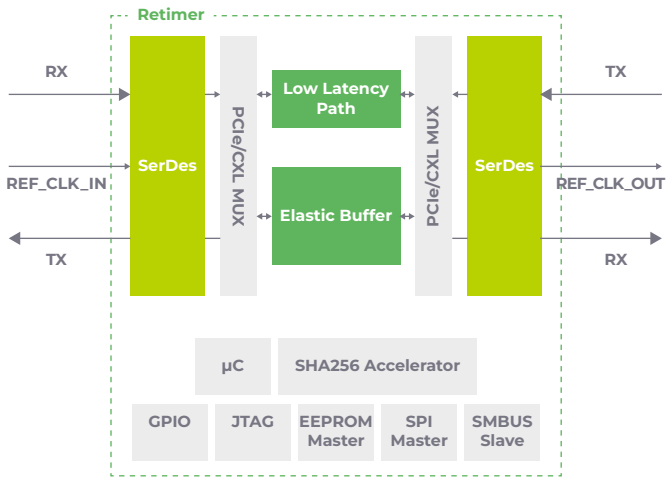
The KB9003 is a 16-lane bidirectional PCIe® 5.0 and CXL™ 2.0 protocol-aware retimer that supports data rates up to 32 GT/s.

Dynamically compensating channel loss up to 36 dB via Kandou's Autonomous Receiver Equalization (ARxE) feature, this retimer allows system designers to increase the PCIe trace length between a root complex and its endpoints, while maintaining signal integrity as per the PCI-SIG specification.

The KB9003 supports:

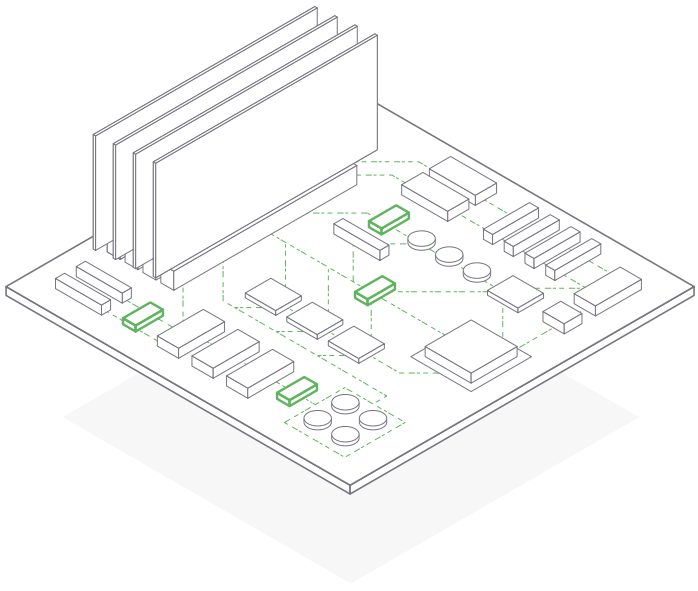
- Compute Express Link™ (CXL) retiming mode. The retimer responds to CXL flex bus capability commands: CXL.io, CXL.mem, CXL.cache and sync header bypass.
- Common clock mode (via an elastic buffer) and SRIS mode with different packet size configuration.
- Drift buffer mode via a low latency datapath that dramatically reduces latency for ultra-low latency applications.

Integrating a microcontroller for a high degree of autonomous operation, the KB9003 operates with minimal system supervision. As this microcontroller is compatible with Kandou's debugging software, system designers can extract runtime telemetry such as EyeScope, BER, and protocol analyzers in real time.



KB9003 Block Diagram

The KB9003 supports PCIe 5.0 and is backward compatible to PCIe 1.0/2.0/3.0/4.0 on main motherboards, midplanes, riser cards, and other application scenarios. It also includes security boot features that prevent attackers from altering its sideband boot configuration stored in external SPI flash or EEPROM.



Features

PCIe 5.0 support

- Supports 2.5, 5, 8, 16, and 32 GT/s:
- Retiming mode: up to MAX packet size (4096 B)
- Common clock mode, SRIS mode
- Ultra-low latency bypass mode
- Link bifurcation support for x16, x8, x4, and x2

CXL 2.0 support

- Sync header bypass
- Enhanced LTSSM to handshake with CXL command
- Drift buffer mode (low latency bypass)

Extended system reach

- RX: Up to 36 dB @ 16 GHz Nyquist using adaptive EQ

Ultra-low latency

- CXL 2.0: 10 ns TYP
- PCIe 5.0 (bypass mode): 10 ns TYP
- PCIe 5.0 (SRIS, 4096 B): 60 ns MAX

Simplified system design

- ARxE, automatic offset calibration, dynamic lane skew compensation, and Advanced Error Reporting (AER).

Ultra-low power consumption

- Power saving state: L1.1(CLK_REQUEST#)
- Power saving mode: VDD_PWR12 (1.2V)

Multiple control interface

- SMBus slave or I2C slave (BMC connection)
- EEPROM master
- SPI master (SPI flash)
- GPIO strapping pins for lane bifurcation configuration
- JTAG

Flexible clock modes

- Integrated clock forward mode buffer
- PCIe REF_CLK IN/OUT (100 MHz)
- SRIS and SRNS mode

Secure boot

- OTP for public key (RSA-2048) storage
- Integrated SHA256 accelerator
- Integrated microcontroller

Integrated debug and error reporting

- Integrated EyeScope
- Integrated BER monitors
- Integrated protocol analyzer
- Multiple loopback modes with PRBS pattern generation

Power supply

- VDD_PWRI: 1.8V
- VDD_PWR12: 1.8V (regular mode), or 1.2V (power saving mode)
- VDD_PWR2: 0.9V

Applications

- Servers, workstations and desktops
- Hyperscalers and data centers
- AI accelerator modules
- 5G infrastructure equipment
- Networking equipment
- PCIe storage
- PCIe riser cards, midplane and backplane
- PCIe active cables

Device information

KB9003-BGA-AR
8.9 x 22.8 mm 354-ball BGA, tape and reel

For ordering or more information, contact sales@kandou.com
www.kandou.com